Switching Characteristics of Nonlinear Field-Effect Transistors: Gallium-Arsenide Versus Silicon

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Abstract—**A study of the switching properties of GaAs FET's and other nonlinear elements whose high field velocity saturates without negative differential mobility demonstrates that the high-bias switching times of GaAs are determined by velocity saturation. Silicon switches are also studied, and situations where GaAs and Si switching properties may be similar are discussed.**

I. Introduction

THE SEMICONDUCTOR gallium-arsenide is a widely used field-effect transistor material. It is an unusual one in that it possesses a region of negative differential mobility (NDM) and two characteristic velocities: a peak velocity prior to the onset of NDM and a saturated drift velocity following the NDM region. The effects of NDM are currently being mapped out and it is developing that NDM separates devices into two categories: those that sustain spontaneous oscillations and those that do not [1]. Devices sustaining spontaneous oscillations, whose origin is due to transiting and recycling space charge layers, generally have cutoff voltages greater than the drain-voltage value at the onset of current saturation. Those that do not, possess cutoff voltages approximately equal to saturation drain voltage. The latter often yield low power and are useful as switching devices. In the last few years there has been an increasing interest in GaAs switches for integrated circuit applications. The advantages for gallium-arsenide are thought to be very high speeds and low-power–delay products. The purpose of this study is to examine these conclusions, and in doing so we highlight the roles that the low field mobility and the high field saturated drift velocity have on the switching times. To place the results in perspective we do similar calculations for the semiconductor silicon.

II. Numerical Simulation Modeling

The switching calculations discussed below are for four different elements, including silicon. For the GaAs FET we examine only those devices that do not sustain spontaneous oscillations. To highlight the importance of the high field drift-velocity values we also present results of calculations with nonlinear elements whose low field mobility is equal to that of gallium-arsenide but whose high field velocity saturates without NDM. In one case the drift velocity saturates to the saturated drift velocity of gallium-arsenide. In the second case it saturates to the peak velocity. The velocity electric-field characteristics for these calculations are displayed in Fig. 1, where we designate the high-saturated drift-velocity element HiV, and the lower saturated drift-velocity element LoV.

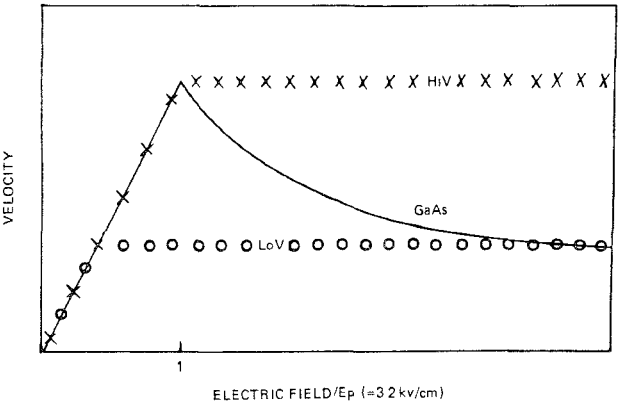

Fig. 1. Drift velocity versus electric-field relation used in the calculations. The gallium-arsenide results are taken from [7, fig. 3].

The calculations with the LoV and HiV elements are more than academic. It is now generally agreed that these nonlinear elements lead to dipole formation within the gate to drain region [2], [3] and that at large values of bias the electrons within this region are traveling at their saturated drift-velocity values. If this is the case then it has been argued that the saturated drift velocity is the primary factor at high-bias levels for determining the switching speeds.

In the following calculation we use an already developed [4] large-signal numerical simulation designed to determine the transient behavior of nonlinear semiconducting FET's. The simulation results in self-consistent solutions to Poisson's equation, the equation of continuity and the external circuit equations. The solutions are for two dimensions plus time with the electrons described by a specific drift velocity versus electric-field curve shown in Fig. 1 and a diffusion electric-field curve shown in Fig. 2.

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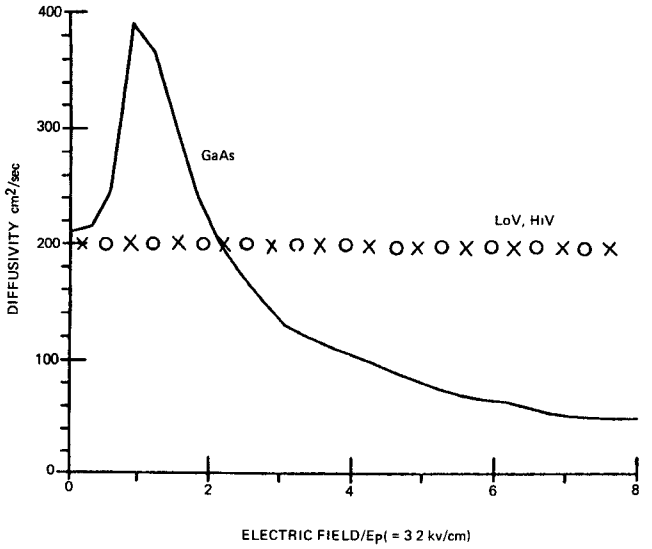

Fig. 2. Diffusivity versus electric field used in the calculations. The gallium-arsenide results are taken from [7, fig. 4].

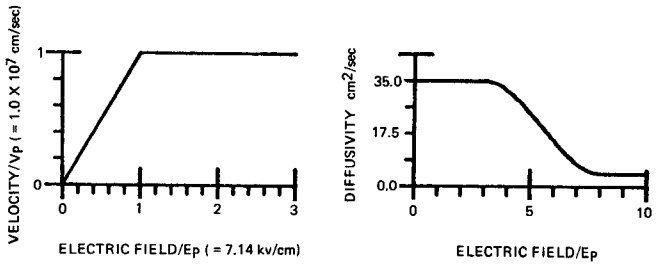

Fig. 3. Silicon parameters used in the calculation. The parameters are adapted from [5].

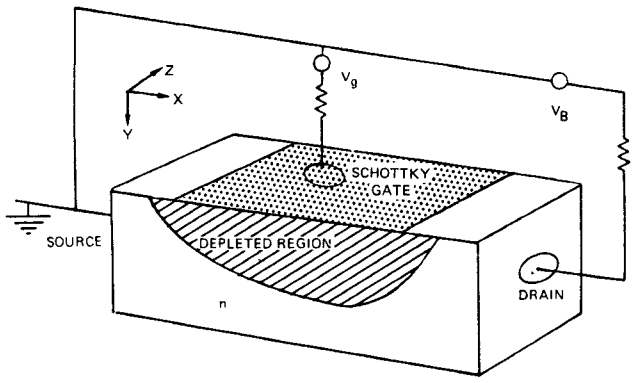

Fig. 4. Schematic representation of a Schottky gate field-effect transistor.

For the silicon calculations the velocity and diffusion field curves [5] are shown in Fig. 3.

The FET device circuit configuration is shown in Fig. 4 and the bulk of our calculations are for $N_0 = 10^{15}/\text{cm}^3$, with the exception of silicon, for which the calculations were done at $5\times10^{15}/\text{cm}^3$. The reason for this difference is discussed below. With regard to Fig. 4 we note that placement of the source and drain regions. In this configuration we concentrate on the physics associated with the space charge and avoid effects due to the geometrical placement of the contacts. The length of the device chosen for the GaAs, LoV, and HiV calculations was 10 μm.

The silicon parameters, which were different from those of the other three elements, were chosen in a way to make the environment as represented by the semiconductor equations, similar for electrons in gallium-arsenide and silicon. For this we concentrated on the equation for total current density for the carriers in the FET:

$$\vec{J} = NeM\vec{E} + eD\,\overrightarrow{\text{grad}}_x N + \epsilon\frac{\partial \vec{E}}{\partial T} \tag{1}$$

where M is the field dependent mobility ($|\vec{V}|/|\vec{E}|$) and D is the field dependent diffusivity, $N(X, Y, T)$ is the mobile carrier density and $\vec{E}(X, Y, Y)$ the electric field, ϵ is the permittivity. We normalize [6] (1), writing it as

$$j = \frac{\vec{J}}{N_0 e V_p} = n\mu\vec{\mathcal{E}} + \left(\frac{L_D}{L_0}\right)^2 \overrightarrow{\text{grad}}_\xi n + \frac{\partial \mathcal{E}}{\partial t} \tag{2}$$

where $t = T/\tau$, $\xi = X/L_0$, $\mathcal{E} = E/E_p$, $\mu = M/M_0$, $L_0 = V_p\tau$, $n = N/N_0$, and

$$L_D = (D\tau)^{1/2} \tag{3}$$

which is a field dependent Debye length . τ is the dielectric relaxation time. At low values of electric field and for a doping level of $10^{15}/\text{cm}^3$, L_D is approximately equal to 0.14 μm for GaAs. Also, in (2), V_p is the peak electron velocity, which for GaAs is approximately 2.2×10^7 cm/s at $10^{15}/\text{cm}^3$, M_0 is the low field mobility, and E_p is the field at V_p. In our simulations we chose the ratio L_D/L_0 to be the same for GaAs and silicon. For this case, at least at low fields, the carriers would find the different semiconductor equations indistinguishable. Differences will occur at high bias levels where the effects of NDM and velocity saturation come into play.

If we use the Einstein relation $D = M_0 k_0 T_0/e$ then the ratio $(L_D/L_0)^2$ is

$$\left(\frac{L_D}{L_0}\right)^2 = \frac{k_0 T_0}{\epsilon}\cdot\frac{N_0}{E_p^2} \tag{4}$$

and for GaAs at $N_0 = 10^{15}$, $E_p = 3.25\times10^3$ V/cm, silicon with $N_0 = 5\times10^{15}/\text{cm}^3$, and $E_p = 7.14\times10^7$ V/cm we find

$$\left(\frac{L_D}{L_0}\right)^2\cdot\frac{\epsilon}{k_0 T_0} = \begin{cases} 0.95\times10^8/\text{V}^2\cdot\text{cm for GaAs} \\ 0.98\times10^8/\text{V}^2\cdot\text{cm for Si} \end{cases} \tag{5}$$

We use these parameters in the simulation.

The normalization associated with (2) is an intrinsic normalization. But the equation for current flow is also subject to boundary condition at the source and the drain contact. To give the carriers the impression that the normalized sample lengths are the same it is necessary to require that the ratio L_{SD}/L_0 be the same for the silicon and gallium-arsenide device. (L_{SD} is the source-to-drain

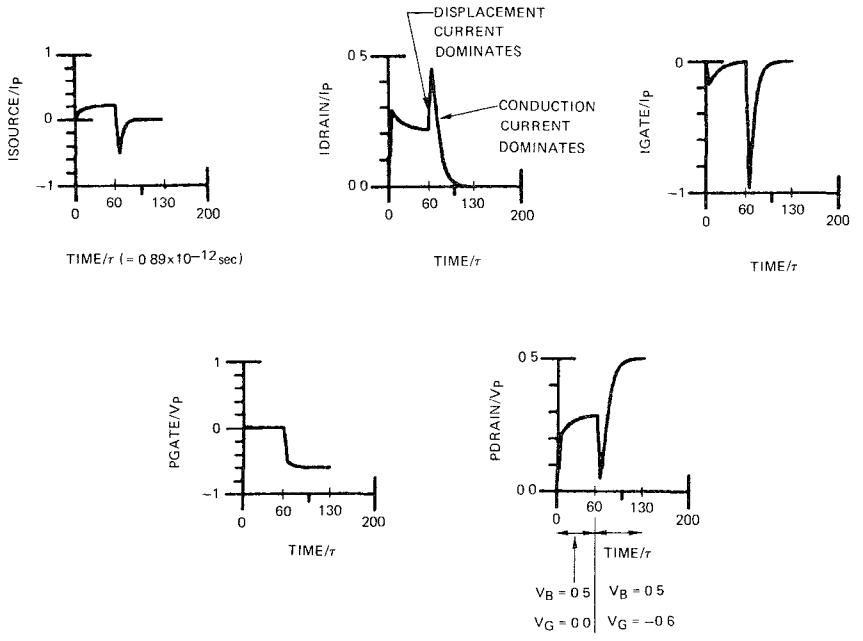

Fig. 5. Time evolution of the current and potential at the three contact for the GaAs FET. The normalization scheme is indicated in the test. Time is in multiples of the dielectric relaxation time.

separation.) The ratio L_{SD}/L_0 is equal to

$$\frac{L_{SD}}{L_0} = \frac{L_{SD}}{V_p \tau} = \frac{L_{SD} N_0}{E_p}\left(\frac{e}{\epsilon}\right) \tag{6}$$

and in the simulation we have chosen $L_{SD} = 4.4$ μm for silicon.

III. Illustrative Calculations

We begin the discussion with the gallium-arsenide element. The output of the simulation is illustrated in the next few figures. In Fig. 5 we display the evolution of the current at the three contacts and the potential at the gate and drain contacts for the situation where, at first the drain bias is increased to 0.5 v_p V($v_p = E_p L_{SD}$) and the gate bias ,s zero. For the second stage the gate bias is decreased relative to ground to the value -0.6 v_p. The bias changes at a finite rate to the values indicated in the figures. The sign conventions are as follows: positive source current denotes current flow into the device through the source contact; positive gate current denotes current flow out of the device through the gate contact; positive drain current denotes current flows out of the device through the drain contact. Thus from Fig. 5 an increase in drain bias results in an increase in drain and source current, with more current leaving the device through the drain current than entering through the source contact. There is a large displacement current with carriers building up on the gate contact. After the initial transient there is a significant conduction current contribution associated with the physical movement of the gate-depletion region until the steady state is reached. The subsequent decrease in gate bias from 0 to -0.6 v_p results in an increase in potential on the drain contact. There is a further buildup of charge on the gate contact and a movement of the depletion layer to the bottom of the device. This effectively cuts off the current flow out of the drain contact. The switching times are estimated from Fig. 5, and in going to the off-state are equal to the magnitude of the difference between the time of initial relaxation and the time at which the drain current reaches a negligible value.

The internal distribution of charge and current associated with the current and potential levels of Fig. 5 is shown in Fig. 6. In Fig. 6(a) we display a set of current density streamlines through the device. The length of each streamline is proportional to the magnitude of the vector current density at the point in question. The maximum length of the individual x and y component before overlap is $J_p = N_0 e V_p$. For the stationary state at 60 τ s in Fig. 5 we see the current density to be greatest under the gate contact as required by current continuity. In Fig. 6(b) we show the current density for the situation where the drain current has been reduced to zero by virtue of the gate bias being set equal to -0.6 v_p. For these GaAs calculations $v_p = 3.2$ V. The density of charged particles within the device is generally nonuniform and Figs. 6(c) and (d) are projections of this distribution. We point out that the particle density increases in the downward direction, and we see the presence of the depletion layer. The position of the gate for these calculations are indicated.

Quantitative estimates of the particle density and potential for the steady-state case at 60τ s are illustrated in Fig. 7, where we display contour plots of these quantities. We note that most of the potential drop is under the gate contact. It is clear that the potential difference between the contours 0.105 v_p and 0.210 v_p are insufficient for the field to reach the threshold for NDM.

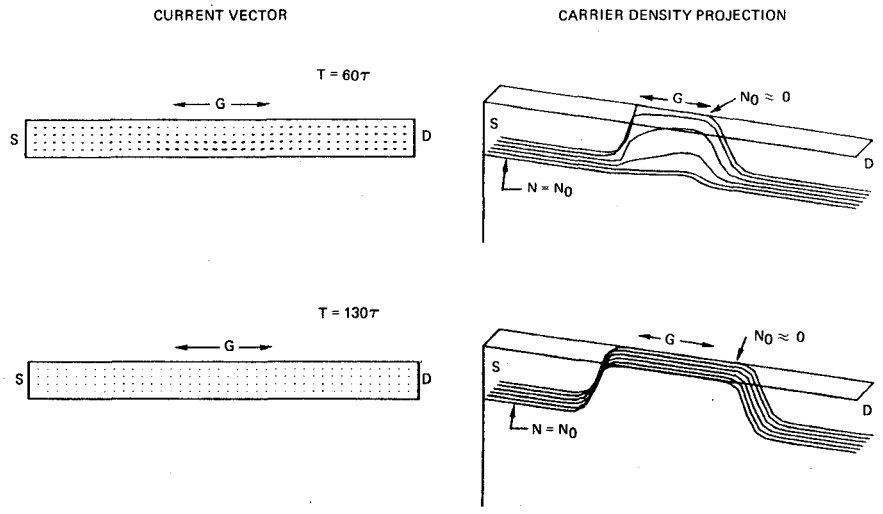

Fig. 6. The internal distribution of current and charge for the parameters of Fig. 5. The time is keyed to the computations of Fig. 5.

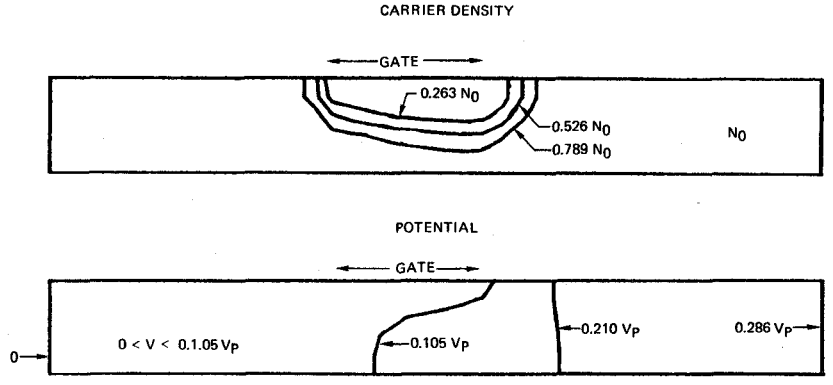

Fig. 7. Contours of charge density and potential for the 60τ s. Calculation of Fig. 5.

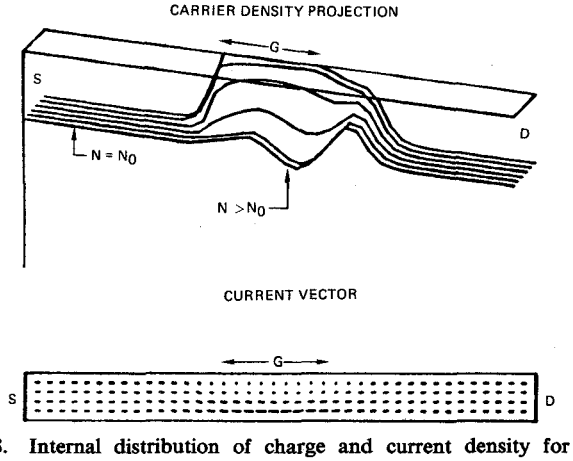

Fig. 8. Internal distribution of charge and current density for the situation where a dipole layer forms under the gate contact. Here $v_B = 1.0v_p$ and $v_G = 0.0$.

An increase in drain bias to v_p results in an increase in potential on the drain contact and a moderate increase in drain current. We are into current saturation. A dipole forms and grows under the gate contact, but there is no current instability. For a 10-μm long device there is about 2 μm of the device within the NDM region. Fig. 8 illustrates with the carrier density projection and current–density vector display. Fig. 9 illustrates with contour plots of potential and carrier density. We have also estimated the average field between the contours of constant potential and find that at the drain side of the gate contact the field exceeds the threshold field for negative differential mobility. The values are indicated in the figure.

As indicated in the introduction, calculations with materials with high field saturated drift velocities also show dipole formation. Fig. 10 illustrates this for silicon, where we show the contour plots of carrier density and potential. The average field under the gate is seen to exceed the critical field of 7 kV/cm. We also show the vector current density display. Here the lines begin to overlap when the current density exceeds $N_0 e V_p$, with V_p equal to 1.0×10^7 cm/s.

IV. Switching Calculations

The above discussion presented the distribution of charge, potential, and current within a device. We next compute the switching properties of the device. We begin by presenting the current–voltage characteristics under zero gate bias conditions for the four simulated elements.

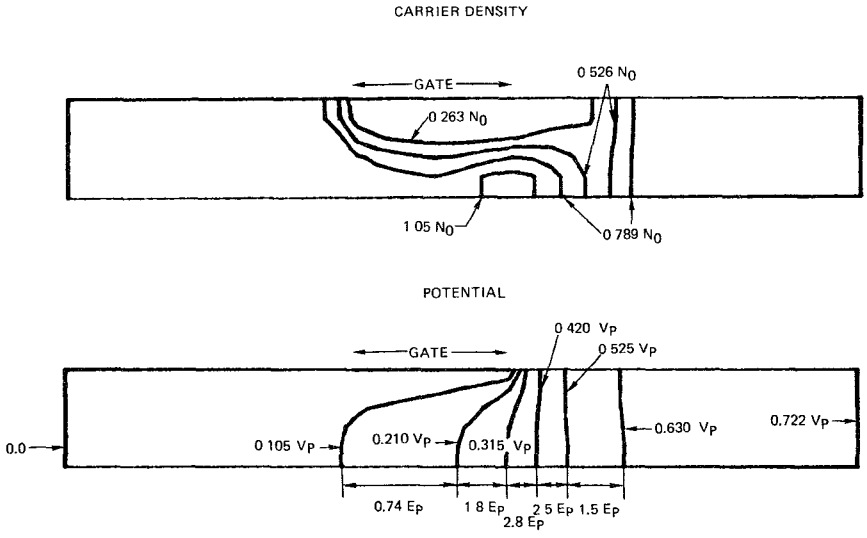

Fig. 9. Carrier density and potential contours for the calculation of Fig. 8. Also shown are estimate of the field between the contours.

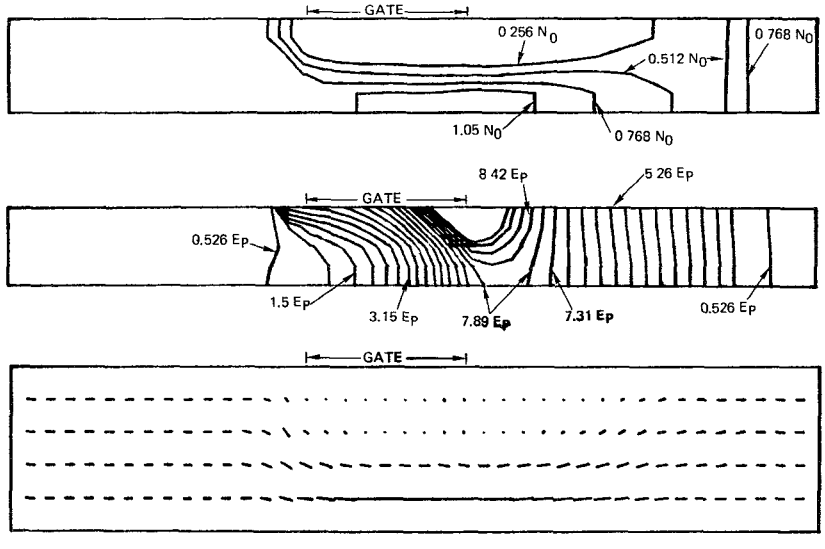

Fig. 10. Contours of carrier density, electric field, and current vector for a three-terminal silicon element showing the presence of a dipole layer under the gate. Here $v_B = 3.0 v_p$, $v_G = 0.0$. The peak field at the *bottom* of the channel occurs between the $7.89 E_p$ contours.

This is displayed in Fig. 11. The current–voltage relation for each element is normalized to I_p and v_p, where $I_p = N_0 e V_p A$ and $v_p = E_p L$. (A is the cross-sectional area in the Y–Z plane.) We note that the simulated points for GaAs are bracketed by those of HiV and LoV, while those for silicon are approximately equal to that for HiV.

In our calculations switching takes place between a point I_D, v_D at zero gate bias and a second point at a level of zero drain current. Both points lie on a dc load line. In the switching process an amount of energy

$$\delta W = \int_{T_1}^{T_2} v_D(T) I_D(T) dT \qquad (7)$$

is transferred. We estimate δW by the power–delay product: $v_D(T_1) I_D(T_1)(T_2 - T_1)$.

The results in Fig. 12 show the power–delay product for the four elements with a load $R = R_0$, where R_0 is the low field resistance of each of the elements. We also show

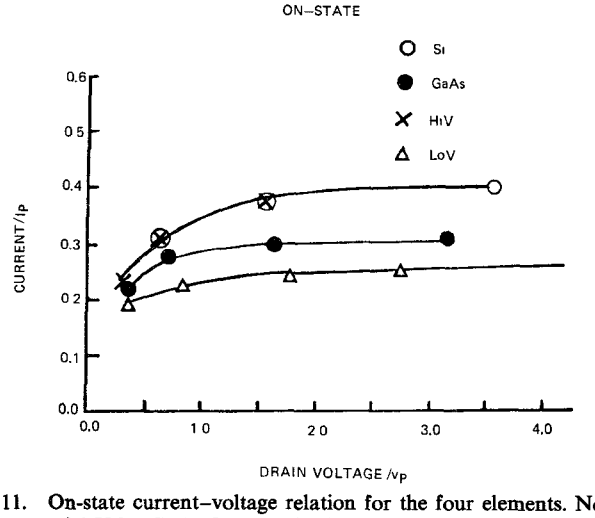

Fig. 11. On-state current–voltage relation for the four elements. Note $v_p = 3.2$ V for GaAs, LoV, and HIV. $v_p = 3.1$ V for silicon.

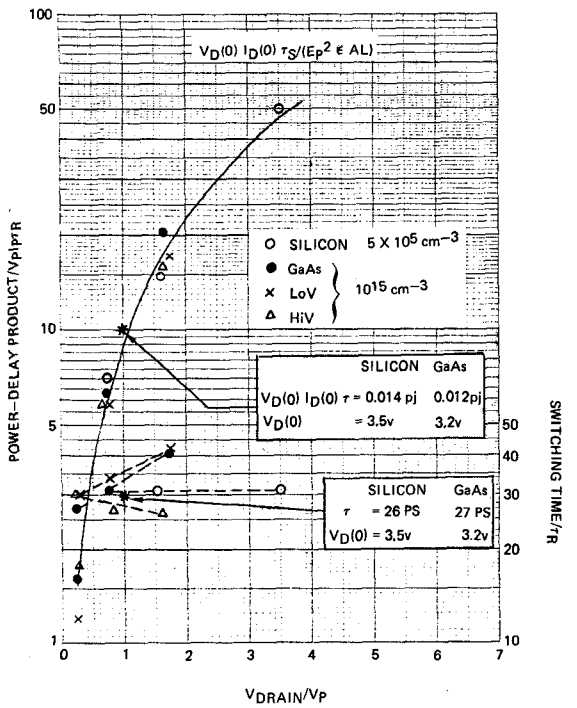

Fig. 12. Normalized power–delay product and normalized switching times versus normalized drain voltage for the four elements used in the calculation.

the switching times normalized to the dielectric relaxation time. Perhaps the most significant feature of this calculation is that GaAs, Lo V, Hi V, and the scaled silicon device all appear to have similar normalized characteristics as far as (7) is concerned. The differences appear in the normalized switching times, with the Hi V being the fastest.

In examining these switching results two extreme situations should be considered: low- and high-bias levels. *At the high-bias* end the GaAs and Lo V element show similar behavior, with both elements displaying longer delay times than that of Hi V. This result provides strong evidence that saturation in the drift velocity of GaAs is the principle determinant of its high-bias switching speed. With regard to the scaled silicon device, its switching times and power delay product are similar to that of Hi V, an element whose mobility is better than four times higher, and whose velocity at saturation is 2.2 times higher. In our calculations the high-bias switching times appear to be determined by the ratio $\hat{L}/V_{sat}$, where $\hat{L}$ represents the length of the high field region. The silicon device has a gate-to-drain spacing that is approximately 1/2 that of Hi V, which may account for the similar switching times.

At low-bias levels we may expect the switching properties to be adequately represented by the Shockley analysis [8] in which case the switching times are proportional to [8], [9] $\tau\ (L/a)^2$ where a is the channel height and τ is the dielectric relaxation time. This result teaches that materials with different mobilities can yield similar delay times, provided their "aspect" ratios and their dielectric relaxation times are similar. The scaling associated with (1)–(6) resulted in comparable values of τ and L/a for all four nonlinear elements. Thus the low-bias switching speeds of all elements should be similar.

Generally, the net switching time of any bias level is composed of several contributions including transit and dielectric relaxation times, parasitic and dissipative load-time constants. It would appear that if the high-bias switching times are determined by velocity saturation and transit through high field regions, than so long as τ is less than the transit time, the value of the doping level will be important only insofar as it influences the field distribution and breakdown conditions. On the other hand, at low-bias levels the switching times will be more sensitive to doping as indicated in the above paragraph.

The above discussion clearly suggests that at high-bias levels similarly designed silicon and gallium FET switches should yield comparable delay times. There are, however, limits to which this result is valid. Continual reduction in the active region length to achieve shorter switching times, will begin to lead to nonequilibrium transient behavior. These transient effects lead to higher transient velocities in gallium-arsenide than in silicon, which should result in shorter switching times for the former. At low-bias levels, but for similar doping, silicon should yield a delay time longer than that of GaAs by the ratio of their mobilities. At intermediate bias levels GaAs should generally be faster than silicon.

With regard to the power–delay product in Fig. 12, it is normalized to the quantity

$$I_p v_p \tau = E_p^2 \epsilon L_x L_y L_z. \tag{8}$$

Now for gallium-arsenide with $L_x = 10$ μm and $L_y = 1.21$ μm

$$I_p v_p \tau = 1.28 \epsilon L_z \qquad \text{(GaAs)}. \tag{9}$$

For the scaling scheme we have used for silicon, with $L_x = 4.4$ μm and $L_y = 0.536$ μm, the normalized products are approximately the same:

$$I_p v_p \tau = 1.20 \epsilon L_z \qquad \text{(silicon)}. \tag{10}$$

Thus for a device whose width is $L_z = 10$ μm, there is a power–delay product, at a normalized drain potential of v_p that for both is approximately equal to 0.012 pJ as indicated in Fig. 12. We note, however that for a silicon and GaAs switch of similar doping and dimensions, low-bias level switching should lead to higher power–delay products for silicon. At bias levels well into saturation they should be more nearly similar.

A recent compilation of data by Greiling [10] on similarly designed GaAs and Si switches shows silicon to have (low-bias) delay times six times longer than that for GaAs. At high-bias levels the switching times of both reflected the fact that the high field carriers were into velocity saturation. Further, at the high-bias levels GaAs was only within a factor of two faster than silicon.

V. Conclusions

The purpose of this study was to examine some of the switching properties of GaAs FET's and to compare them to silicon FET's. The results demonstrate that at high-bias levels the delay time of GaAs is determined by velocity saturation. Further so long as nonequilibrium effects may

be ignored, switching speeds for GaAs and silicon will be similar for comparably designed structures operated at high-bias levels. (This latter conclusion ignores differences in parasitic contributions.) At low-bias levels, scaling principles indicate the silicon delay times will be longer than those of gallium-arsenide by the ratio of their mobilities. Intermediate fields will result in shorter delay times for gallium-arsenide.

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A MESFET Model for Use in the Design of GaAs Integrated Circuits

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Abstract—**A MESFET model is presented that is suitable for use in conventional, time-domain circuit simulation programs. The parameters of the model are evaluated either from experimental data or from more detailed device analysis. The model is shown to be more complete than earlier models, which neglect transit-time and other effects. An integrated circuit (IC) design example is discussed.**

I. Introduction

THE PURPOSE of this paper is to present a reasonably simple analytical model for the GaAs MESFET that is appropriate for use in circuit simulation programs. A number of presently available models will be reviewed and criteria for accurate modeling will be presented. Several examples of logic circuit simulation will be described.

The design and development of GaAs integrated circuits (IC's) is aided considerably if circuits may be studied using high-speed computers. Many large computer programs are available for studying dc and transient characteristics of complex combinations of transistors, resistors, capacitors and inductors. However, the success of the mathematical simulation depends totally on the accuracy of the mathematical model. The model must reflect the exact physical properties of the circuit.

The difficulty with MESFET devices is that they are extremely complex internally and simple external models cannot accurately describe their behavior under all conditions. Conversely, a detailed two-dimensional (internal) model [1]–[4] of the device, although more accurate, is not suitable for use with circuit simulation programs.

One approach is to then develop an external characterization of the particular MESFET devices used in the circuit under study. That is, the model used will not attempt to be complete enough for all ranges of device parameters.

A number of MESFET models can be found in the literature. Madjar and Rosenbaum [5] utilize the two-dimensional model of Yamaguchi and Kodera [3] to produce analytical relationships for drain and gate currents as a function of drain–source voltage, gate–source voltage, and their derivatives. This approach appears useful for studying the interaction between the device with its parasitics and its external circuits, such as in frequency multiplier operation. However, the technique would not

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